AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended): A method of testing a silicon-on-insulator (SOI) wafer comprising:

(a) providing an SOI wafer having an insulating layer sandwiched between a semiconductor top layer and a semiconductor substrate;

(b) moving a pair of spaced, elastically deformable contacts and a surface of the SOI wafer exposed on a side thereof opposite the semiconductor substrate into contact;

(c) applying a first voltage to the semiconductor substrate;

(d) applying a second voltage to at least one of the ~~probes~~ contacts;

(e) sweeping at least one of the first voltage and the second voltage from a first value toward a second value;

(f) measuring a current that flows in the SOI wafer in response to the sweep of the at least one voltage; and

(g) determining at least one characteristic of the SOI wafer as a function of the measured current flow and the at least one voltage.

2. (original): The method of claim 1, wherein at least one of the first voltage and the second voltage is a DC voltage.

3. (original): The method of claim 1, wherein at least one of the first voltage and the second voltage is a reference voltage.

4. (original): The method of claim 1, wherein the surface of the SOI wafer is a dielectric overlaying a surface of the semiconductor top layer.

5. (currently amended): The method of claim 1, wherein the second voltage is applied between the ~~probes~~ contacts.

6. (original): The method of claim 1, wherein step (g) further includes:

measuring a voltage of the semiconductor top layer; and

utilizing the measured voltage to determine the at least one characteristic of the SOI wafer.

7. (original): The method of claim 1, wherein the at least one characteristic includes at least one of:

a threshold voltage;

carrier mobility in the semiconductor top layer;

conduction factor of the semiconductor top layer;

trap density of an interface between the insulating layer and the semiconductor top layer;

dopant density of the semiconductor top layer; and

generation lifetime of the semiconductor top layer.

8. (currently amended): The method of claim 1, wherein at least ~~the~~ a portion of each elastically deformable contact in contact with the semiconductor top layer is formed from one of tantalum, platinum and iridium.

9. (original): A method of testing a silicon-on-insulator (SOI) wafer comprised of an insulating layer sandwiched between a semiconductor top layer and a semiconductor substrate, the method comprising:

(a) causing a pair of spaced conductors to contact a surface of the SOI wafer exposed on a side thereof opposite the semiconductor substrate;

(b) applying a first bias to the semiconductor substrate and a second bias to at least one of the conductors;

(c) sweeping one of the first bias and the second bias from a first value toward a second value;

(d) measuring current flowing in the SOI wafer during the sweep of the at least one bias; and

(e) determining at least one characteristic of the SOI wafer from the measured current as a function of the at least one swept bias.

10. (original): The method of claim 9, wherein at least one of the first bias and the second bias is a DC voltage.

11. (original): The method of claim 9, wherein at least one of the first bias and the second bias is a reference voltage.

12. (original): The method of claim 9, wherein:

the SOI wafer includes a dielectric disposed on a surface of the semiconductor top layer facing opposite the semiconductor substrate; and

the pair of conductors contact the dielectric.

13. (original): The method of claim 9, further including measuring a voltage of the semiconductor top layer and utilizing the measured voltage to determine the one characteristic of the SOI wafer.

14. (original): The method of claim 9, wherein the at least one characteristic includes at least one of:

a threshold voltage;

carrier mobility in the semiconductor top layer;

conduction factor of the semiconductor top layer;

trap density of an interface between the insulating layer and the semiconductor top layer;

dopant density of the semiconductor top layer; and

generation lifetime of the semiconductor top layer.

15. (original): The method of claim 9, further including:

positioning a surface of the semiconductor substrate facing opposite the insulating layer on a surface of an electrically conductive chuck; and

applying the first bias to the chuck whereupon the first bias is applied to the semiconductor substrate.